IN THE CLAIMS

Please cancel claims 6, 12, 13, and 20-23.

Please amend claims 2-5, 7, 14, 15, 17, and 18 as follows:

1. (Cancelled)

2. (Currently Amended) The multi-chip package of claim ~~6~~7, wherein the memory device comprises a random access memory device.

3. (Currently Amended) The multi-chip package of claim ~~6~~7, wherein the memory device comprises a magnetic random access memory device.

4. (Currently Amended) The multi-chip package of claim ~~6~~7, wherein the logic device comprises a microprocessor.

5. (Currently Amended) The multi-chip package of claim ~~6~~7, wherein the temperature signal is indicative of a junction temperature of the memory device.

6. (Cancelled)

7. (Currently Amended) ~~The multi-chip package of claim 6,~~ A multi-chip package comprising:

a memory device receiving a clock signal having a frequency, the memory device operating at the clock signal frequency and including a temperature sensor providing a temperature signal representative of a temperature of the memory device, wherein the memory device has a rated operating frequency at a rated operating temperature; and

a logic device providing the clock signal and receiving the temperature signal, wherein the logic device adjusts the clock signal frequency based on the temperature signal, and wherein

the logic device provides the clock signal at a first frequency when the temperature signal indicates that the temperature of the memory device is less than a threshold temperature, and provides the clock signal at a second frequency when temperature signal indicates that the temperature of the memory device is at least equal to the threshold temperature, wherein the threshold temperature is substantially equal to rated operating temperature, wherein the first frequency is substantially equal to the rated operating frequency, and wherein the second frequency is less than the first frequency and at a frequency at which the memory device operates reliably at a temperature above the rated operating temperature.

8. (Original) The multi-chip package of claim 7, wherein the logic device further includes a clock generator configured to generate the clock signal.

9. (Original) The multi-chip package of claim 8, wherein the temperature sensor provides the temperature signal having a first state when the temperature of the memory device is less than rated operating temperature and having a second state when the temperature of the memory device is at least equal to the threshold temperature, and wherein the wherein the clock generator provides the clock signal at the rated operating frequency when the temperature signal has the first state and at the second frequency when the temperature signal has the second state.

10. (Original) The multi-chip package of claim 8, wherein the logic device further includes a memory controller configured to control access operations of the memory device by the logic device, wherein the temperature sensor provides the temperature signal in response to a read signal, wherein the memory controller provides the read signal and provides a flag signal having a first state when the temperature signal indicates that the memory device temperature is less than the rated operating temperature and a second state when the temperature signal indicates that the memory device temperature is at least equal to the rated operating temperature, and wherein the wherein the clock generator provides the clock signal at the rated operating frequency when the flag signal has the first state and at the second frequency when the flag signal has the second state, and wherein the memory controller provides a wait signal

representative of whether an access operation is on-going, and wherein a timing of an adjustment of the clock signal frequency by the clock generator is based on the wait signal.

11. (Cancelled)

12. (Cancelled)

13. (Cancelled)

14. (Currently Amended) ~~The clock system of claim 13,~~ A clock system in a multichip package including a memory device, the clock system comprising:

a clock generator providing a clock signal having a frequency to the memory device, wherein the memory device has a rated operating frequency at a rated operating temperature; and

a temperature sensor providing a temperature signal representative of a temperature of the memory device, wherein the clock generator adjusts the frequency of the clock signal based on the temperature signal, and wherein the clock generator provides the clock signal at a first frequency when the temperature signal indicates that the temperature of the memory device is less than a threshold temperature and at a second frequency when the temperature signal indicates that the temperature of the memory device is at least equal to the threshold temperature; wherein the threshold temperature is substantially equal to the rated operating temperature, wherein the first frequency is substantially equal to the rated operating frequency, and wherein the second frequency is less than the first frequency and at a frequency at which the memory device operates reliably at a temperature above the rated operating temperature.

15. (Currently Amended) The clock system of claim ~~12~~14, wherein multichip package includes a logic device.

16. (Original) The clock system of claim 15, wherein the logic device comprises a microprocessor.

17. (Currently Amended) The clock system of claim ~~12~~14, wherein the memory device comprises a random access memory device.

18. (Currently Amended) The clock system of claim ~~12~~14, wherein the memory device comprises a magnetic random access memory device.

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Cancelled)

23. (Cancelled)